Gonzalo Carvajal Barrera

Curriculum Vitae

✉ *e-mail (gcarvaja@uwaterloo.ca, gcarvajalb@gmail.com)*

Education

2013 **Ph.D., Electrical Engineering**, *Universidad de Concepción*, Chile.
Thesis: "Network Devices for Hard Real-Time Communication on Switched Ethernet". In collaboration with the University of Waterloo, ON, Canada.

2009 **M.Sc., Electrical Engineering**, *Universidad de Concepción*, Chile.
Thesis: "Analysis and Compensation of the Effects of Analog-VLSI Arithmetic in Linear Subspace-based Face Recognition Systems".

2006 **Electronics Engineer**, *Universidad de Concepción*, Chile.

Research Experience

Mar. 2014 – May 2015 **Postdoctoral Associate**, *Carnegie Mellon University*, PA, USA.
Electrical and Computer Engineering (ECE) Department. Member of the System Level Design Group (http://www.ece.cmu.edu/~sld)

Aug. 2013 – Feb. 2014 **Postdoctoral Fellow**, *University of Waterloo*, ON, Canada.
ECE Department. Member of the Real-Time Embedded Systems Group (http://esg.uwaterloo.ca)

Jan. 2012 – Jul. 2013 **Research Assistant**, *University of Waterloo*, ON, Canada.
ECE Department. Member of the Real-Time Embedded Systems Group (http://esg.uwaterloo.ca)

2008 **Research Internship**, *University of Waterloo*, ON, Canada.
Visiting researcher at the Real-Time Embedded Systems Group (http://esg.uwaterloo.ca)

2005 – 2012 **Research Assistant**, *Universidad de Concepción*, Chile.
Department of Electrical Engineering (DIE). Participating in multiple projects funded through Chilean agencies.

Teaching and Mentoring

2012 – present **Student Supervision**.
Supervising research and engineering projects for students participating in the following programs:

- Undergrad co-ops and Undergraduate Research Assistants (URA), University of Waterloo.
- Visiting graduate students, University of Waterloo.
- Undergraduate Research Opportunities (URO), Carnegie Mellon University.

2007 and 2009–2010 **Lecturer**, *Universidad de Concepción*, Chile.
Duties included renovation of course contents, evaluation scheme, and acquisition and adoption of new tools and laboratory equipment for the following courses at the DIE: Algorithms and Programming Languages, Digital Systems, and Computers Laboratory.

2001–2006 **Teaching Assistant**, *Universidad de Concepción*, Chile.
Multiple undergraduate and graduate level courses at the DIE and Faculty of Physics and Mathematics.

Honors and Awards

2012 **MECESUP for International Research Stays**, *Chilean Government*, Chile.
Covered stipend for a research internship at the University of Waterloo, ON, Canada

2008 **GSEP for Research Internships in Canada**, *Canadian Government*, Canada.
Covered travel and stipend for a research internship at the University of Waterloo, ON.

2008 **CONICYT Scholarship for Graduate Studies**, *Chilean Government*, Chile.
Full coverage of tuition and stipend during the Ph.D. program.

2006 **Ranked 1st of the Class**, *Universidad de Concepción*, Chile.
Obtained the professional degree in Electronic Engineering with highest distinction.

1999 **Enrique Molina Scholarship**, *Universidad de Concepción*, Chile.
Highest scholarship granted by the Universidad de Concepción. Full coverage of tuition and stipend during the undergrad program.

Extracurricular Volunteering and Outreach Activities

Previous.

- Volunteer work through different organizations (Summer Volunteering Jobs, Techos para Chile) servicing impoverished suburban areas and remote rural locations in Chile.
- Active role in reconstruction campaigns for the Universidad de Concepcion's facilities after the 2010's earthquake in Chile.

Current.

- Leading an independent alumni organization funding scholarships for undergrad students from low-income families at the Universidad de Concepción.
- Always interested on dissemination of science and technology to the general public, particularly in primary and high-schools.

Relevant Publications

Journals

[1] **G. Carvajal** and M. Figueroa, "Model, analysis, and evaluation of the effects of analog VLSI arithmetic on linear subspace-based image recognition," *Neural Networks*, vol. 55, pp. 72–82, 2014.

[2] **G. Carvajal**, C. Wu, and S. Fischmeister, "Evaluation of communication architectures for switched real-time Ethernet," *IEEE Transactions on Computers*, vol. 63, no. 1, pp. 218–229, 2014.

[3] **G. Carvajal**, M. Figueroa, D. Sbarbaro, and W. Valenzuela, "Analysis and compensation of the effects of analog-VLSI arithmetic on the LMS algorithm," *IEEE Transactions on Neural Networks*, vol. 22, no. 7, pp. 1046–1060, 2011.

[4] W. Valenzuela, **G. Carvajal**, and M. Figueroa, "Blind source separation in mixed-signal VLSI," *Neural Network World*, vol. 19, no. 5, pp. 641–656, 2009.

Conference Proceedings

[5] A. Azim, **G. Carvajal**, R. Pelizzoni, and S. Fischmeister, "Generation of communication schedules for multi-mode distributed real-time applications," in *Proc. of the Design, Test, and Automation in Europe Conference (DATE)*, Mar. 2014.

[6] **G. Carvajal**, M. Figueroa, R. Trausmuth, and S. Fischmeister, "Atacama: an open FPGA-based platform for mixed-criticality communication in multi-segmented Ethernet networks," in *Proc. of the IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Apr. 2013.

[7] **G. Carvajal** and S. Fischmeister, "An open platform for mixed-criticality real-time Ethernet," in *Proc. of the Design, Test, and Automation in Europe Conference (DATE)*, Mar. 2013.

[8] J. Moreno, R. Redlich, **G. Carvajal**, and M. Figueroa, "Hardware-based computation of the roughness index for infrared imagers," in *VIII Southern Conference on Programmable Logic (SPL)*, Mar. 2012, 1–6 (*Best Paper Award*).

[9] R. Redlich, **G. Carvajal**, and M. Figueroa, "An FPGA-based real-time nonuniformity correction system for infrared focal plane arrays," in *Proc. of the 22nd IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP)*, Sep. 2011, pp. 202–208.

[10] **G. Carvajal** and S. Fischmeister, "A TDMA Ethernet switch for dynamic real-time communication," in *Proc. of the IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 2010, pp. 119–126.

[11] **G. Carvajal**, M. Figueroa, and W. Valenzuela, "Image recognition in analog VLSI with on-chip learning," *Springer-Verlag Lecture Notes in Computer Science*, no. 3697, pp. 429–438, Sep. 2009.

[12] W. Valenzuela, **G. Carvajal**, and M. Figueroa, "Blind source separation in mixed-signal VLSI using the Infomax algorithm," *Springer-Verlag Lecture Notes in Computer Science*, no. 5164, pp. 208–217, Sep. 2008.

[13] **G. Carvajal**, W. Valenzuela, and M. Figueroa, "Subspace-based face recognition in analog VLSI," in *Advances in Neural Information Processing Systems 20*, 2007, pp. 133–140.

[14] **G. Carvajal**, M. Figueroa, and S. Bridges, "Effects of analog-VLSI hardware on the performance of the LMS algorithm," *Springer-Verlag Lecture Notes in Computer Science*, no. 4131, pp. 963–973, Sep. 2006.

[15] M. Figueroa, E. Matamala, **G. Carvajal**, and S. Bridges, "Adaptive signal processing in mixed-signal VLSI with anti-hebbian learning," in *Proc. of the 2006 IEEE Computer Society Annual Symposium on VLSI*, 2006, pp. 133–140.

[16] D. Sbarbaro and **G. Carvajal**, "Supervision of control valves in flotation circuits based on artificial neural networks," *Springer-Verlag Lecture Notes in Computer Science*, no. 3697, pp. 451–456, Sep. 2005.

Additional Academic Activities

Tutorials

[1] **G. Carvajal** and S. Fischmeister, "Atacama: an open research platform for mixed-criticality real-time switched Ethernet," in *Cyber-Physical Systems (CPS) Week*, Apr. 2013.

Demonstration Sessions

[1] D. Arney, S. Fischmeister, J. Goldman, **G. Carvajal**, and R. Trausmuth, "Plug-and-play for networked medical devices: a case study on Patient Controlled Analgesia," in *Center for Integration of Medicine and Innovative Technology - CIMIT Innovation Congress*, Oct. 2008.

[2] **G. Carvajal** and S. Fischmeister, "An open experimental platform for real-time Ethernet," in *Real-Time Systems Symposium*, Dec. 2012.

[3] **G. Carvajal**, S. Fischmeister, M. Figueroa, and R. Trausmuth, "Atacama: an open FPGA-based platform for mixed-criticality communication in multi-segmented Ethernet networks," in *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM) - Demo Night*, May 2013.

[4] **G. Carvajal** and S. Fischmeister, "Atacama: an open experimental platform for mixed-criticality networking on top of Ethernet," in *Real-Time Systems Symposium*, Dec. 2013.

[5] **G. Carvajal**, "Hardware-in-the-loop technology for advanced debugging and testing: a case study on an Scalable Deposit Module," in *Report on Engage Grants between Univeristy of Waterloo and NCR Corporation*, Dec. 2013.

Recent Peer-review

- IEEE Transactions on Computers
- IEEE Transactions on Neural Networks and Learning Systems
- IEEE Design and Test
- IEEE Transactions on Multi-Scale Computing Systems
- IEEE Transactions on Control Systems Technology
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
- ACM Journal of Emerging Technologies in Computing Systems
- ACM Transactions on Embedded Computing Systems
- Springer's Real-Time Systems Journal
- IEEE Real-Time Systems Symposium (RTSS)
- IEEE Real-Time, Embedded Technology and Applications Symposium (RTAS)
- Conference on Design, Test, and Automation in Europe (DATE)
- IEEE Conference on Emerging Technologies and Factory Automation (ETFA)
- Euromicro Conference on Digital Systems Design (DSD)
- International Conference on Languages, Compilers and Tools for Embedded System (LCTES)
- IEEE Conference on Cyber-Physical Systems, Networks and Applications (CPSNA)
- International Symposium on Networks on Chip (NOCs)